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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PE, MARK D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,235	SHIMIZU, KAZUHIRO	
	Examiner	Art Unit	
	Mark D. Pe	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/24/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1) Applicant's election with traverse of claims 1-11 in the reply filed on 09/16/2005 is acknowledged. The traversal is on the ground(s) that:

"Applicant traverses the outstanding Restriction requirement on the grounds that it has not been established that it be an undue burden to examine each of the noted inventions and claims together."

This is not found persuasive because:

A burden is established when an invention is classified under separate classifications. (See MPEP 808.02)

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2) Claim 2 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, claim 1 defined a first trench isolation structure and claim 2 re-defined it. It is unclear to which is the first trench isolation structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3) Claim 1, 2 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent Application Laid-Open No. 9-283716 (1997) in view of Wada (US 0.6274919).

With respect to claim 1, Japanese Patent Application Laid-Open No. 9-283716 (1997) discloses in Figure 12, "A semiconductor device comprising:

a semiconductor substrate (1) of a first conductivity type (p);

a semiconductor layer (2) of a second conductivity type (n) provided on said semiconductor substrate (1);

a first impurity region (3) of said first conductivity type (p) provided in said semiconductor layer (2), extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate (1), said first impurity region (3) defining a RESURF isolation region;

a semiconductor element (RESURF: 8, 5 & 6) provided in said semiconductor layer (2) defined in said RESURF isolation region; and

a first MOS transistor (nch RESURF MOS), comprising

a second impurity region (5) of said second conductivity type (n) provided in said upper surface of said semiconductor layer, said second impurity region (5) being connected to a drain electrode (8) of said first MOS transistor (NCH RESURF MOS),

a third impurity region (nch RESURF MOS: 6) of said first conductivity type (p) provided in said upper surface of said semiconductor layer defined between said first (3) and second (5) impurity regions, and

a first source region (nch RESURF MOS: 5) of said second conductivity type provided in an upper surface of said third impurity region (nch RESURF MOS: 6),

wherein said semiconductor device further comprises a buried layer region (4) of said second conductivity type (n) provided under said second impurity region (5) and at said interface between said semiconductor layer (2) and said semiconductor substrate (1), said buried impurity region being higher in impurity concentration (n+) than said semiconductor layer (n-)."

Japanese Patent Application Laid-Open No. 9-283716 (1997) was silent on a first trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region (RESURF IR) to be connected to said first impurity region (3), extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said first trench isolation structure and said first impurity region together defining a first trench isolation region in said RESURF isolation region.

Wada (US 6274919) teaches an isolation approach called field-shield device isolation (FSDI). The FSDI method relates to a MOS structure for separating devices by

forming a field-shield insulator film and a field-shield electrode between two active regions of the device. By fixing the field-shield electrode potential at a reference potential (e.g. GND or 0V), the formation of parasitic channels on the device surface is prevented, thereby providing insulative isolation of the active regions of the devices (Col. 1: lines 31-40).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to take the teaching of Wada (US 6274919) of using an insulated conductive trench (FDSI) and incorporate it in the invention of the Japanese Patent Application Laid-Open No. 9-283716 (1997) to attain a field-shield structure having a potential reference of GND thereby preventing the formation of the parasitic channels to provide an effective insulative isolation between active regions (Col. 1: lines 31-40).

With respect to claim 2, Japanese Patent Application Laid-Open No. 9-283716 (1997) was silent on further comprising a second trench isolation structure separated by a certain distance from said first trench isolation structure, said second trench isolation structure being provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure, said first impurity region, and said first trench isolation structure together defining said first trench isolation region in said RESURF isolation region.

As discussed in claim 1, a first trench isolation structure is formed on the first impurity region (3 – the 3 on the left side as seen on figure 12).

The Japanese Patent Application Laid-Open No. 9-283716 (1997) also teaches a top view layout in Figure 1 of the nch Resurf MOSFET and the RESURF region. A grid or a guard ring is shown around the nch RESURF MOSFET area for isolation purposes.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of the Japanese Patent Application Laid-Open No. 9-283716 (1997) as shown in Figure 1, the teaching of Wada and the structure of claim 1 to form a trench type guard ring to attain a field-shield structure having a potential reference of GND thereby preventing the formation of the parasitic channels to provide an effective insulative isolation between active regions (Wada: Col. 1: lines 31-40).

With respect to claim 6, Japanese Patent Application Laid-Open No. 9-283716 (1997) was silent on wherein said first trench isolation structure reaches said semiconductor substrate, and

wherein an end portion of said first trench isolation structure reaches a depth shallower than the greatest possible depth of said buried impurity region.

Referring to the Japanese Figure 12 and the discussion as describe in claim 1 above, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the isolation structure to the claimed depth to attain a field-shield structure having a potential reference of GND (touching the substrate) thereby preventing the formation of parasitic channels (touching the greatest depth will destroy the function of the PN isolation given by the buried impurity region) to provide effective insulative isolation between active regions (Wada: Col. 1: lines 31-40).

4) Claim 3-5 and 7-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent Application Laid-Open No. 9-283716 (1997) in view of Wada (US 6274919) and further in view of Leonardi (US 2002/0008299).

With respect to claim 3, Japanese Patent Application Laid-Open No. 9-283716 (1997) was silent on wherein said first trench isolation structure comprises an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of space-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of first insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer.

The Japanese Patent Application Laid-Open No. 9-283716 (1997) also teaches a top view layout in Figure 1 of the nch Resurf MOSFET and the RESURF region. A grid or a guard ring is shown around the nch RESURF MOSFET area for isolation purposes.

Leonardi (US 2002/0008299) teaches that it is known in the art to use junction isolation (reverse bias condition of the P-N junction) as isolation between components. Also, capacitive and/or inductive effects, due either to the presence of several layers or the type of bias applied, make the electrical isolation of the integrated components uncertain (paragraph: 007). Leonardi also teaches a plurality of insulated conductive trenches uses the insulative part being a dielectric which removes all of the parasitic

effects due to the effects mentioned above and using the trench isolation structure to provide a more reduced size due to it takes less space to do a trench isolation versus doing a junction isolation. Also the trench isolation structure will act as interfacing regions, thereby enabling the device to serve a number of electrical functions without involving any special logical or circuit solutions (paragraph: 0042-0045). The conductive filler makes it able to connect to the lower regions from the surface (paragraph: 0027). Also, to extend the plurality of trench isolation structures to extend over a larger area, thus making for lower contact resistance (paragraph: 0066).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Leonardi (US 2002/0008299), the Japanese Patent Application Laid-Open No. 9-283716 (1997) in Fig. 1 and the structure as discussed in claim 1 to formed the claimed structure (using the Japanese Application Figure 1 guard ring as reference to the in-line portion) to attain an isolation structure which has a reduced area requirements and improved electrical isolation of the integrated components in the isolation wells and the isolation structure suiting any (low- and high-voltage) semiconductor devices provided with isolation wells that have been formed by the junction isolation technique (paragraph: 0026).

With respect to claim 4, Japanese Patent Application Laid-Open No. 9-283716 (1997) was silent on wherein the openings between adjacent ones of said plurality of conductive films are filled with said plurality of first insulating films.

Leonardi (US 2002/0008299) also teaches that two adjoining trenches may be formed with different aperture and spacings, such that the oxidized regions in the sidewell (of the trenches) will join together (paragraph: 0053-0054 and 0068).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to take the teaching of Leonardi (US 2002/0008299) and combine it with the claimed structure of claim 3 to fill openings of the conductive films with insulation for optimization purposes.

With respect to claim 5, Japanese Patent Application Laid-Open No. 9-283716 (1997) was silent on wherein said first and second trench isolation structures each comprise an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of space-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer.

Leonardi (US 2002/0008299) teaches that it is known in the art to use junction isolation (reverse bias condition of the P-N junction) as isolation between components. Also, capacitive and/or inductive effects, due either to the presence of several layers or the type of bias applied, make the electrical isolation of the integrated components uncertain (paragraph: 007). Leonardi also teaches a plurality of insulated conductive

trenches uses the insulative part being a dielectric which removes all of the parasitic effects due to the effects mentioned above and using the trench isolation structure to provide a more reduced size due to it takes less space to do a trench isolation versus doing a junction isolation. Also the trench isolation structure will act as interfacing regions, thereby enabling the device to serve a number of electrical functions without involving any special logical or circuit solutions (paragraph: 0042-0045). The conductive filler makes it able to connect to the lower regions from the surface (paragraph: 0027). Also, to extend the plurality of trench isolation structures to extend over a larger area, thus making for lower contact resistance (paragraph: 0066).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Leonardi (US 2002/0008299) and apply it to the Japanese Patent Application Laid-Open No. 9-283716 (1997) structure of claim 2 and form the claimed structure above (Using Japanese figure 1 as reference for a plan view: the first trench will follow the 2b direction and the second trench will follow the 2a direction) to attain an isolation structure which has a reduced area requirements and improved electrical isolation of the integrated components in the isolation wells and the isolation structure suiting any (low-and high-voltage) semiconductor devices provided with isolation wells that have been formed by the junction isolation technique (paragraph: 0026).

With respect to claim 7, Japanese Patent Application Laid-Open No. 9-283716 (1997) was silent on wherein said first trench isolation structure comprises an in-line

portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of spaced-apart insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer, and

wherein said semiconductor device further comprises a fourth impurity region provided in said upper surface of said semiconductor layer defined in said RESURF isolation region, surrounding each one of said plurality of insulating films while filling openings between adjacent ones of said plurality of insulating films.

Leonardi (US 2002/0008299) teaches the trench isolation structure will act as interfacing regions between several close wells or from edge regions, thereby enabling the device to serve a number of electrical functions without involving any special logical or circuit solutions (paragraph: 0045).

Leonardi (US 2002/0008299) also teaches that it is known in the art to use junction isolation (reverse bias condition of the P-N junction) as isolation between components. Leonardi also teaches a plurality of insulated conductive trenches uses the insulative part being a dielectric which removes all of the parasitic effects due to the effects mentioned above and using the trench isolation structure to provide a more reduced size due to it takes less space to do a trench isolation versus doing a junction isolation (paragraph: 0042-0044). The conductive filler makes it able to connect to the

lower regions from the surface (paragraph: 0027). Also, to extend the plurality of trench isolation structures to extend over a larger area, thus making for lower contact resistance (paragraph: 0066).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to take the teaching of Leonardi (US 2002/0008299) and combine it with the structure of claim 1 to form the claimed structure (utilizing the common knowledge of a P-N junction from the definition above to form the fourth impurity surrounding the plurality of insulating films), to act as interfacing regions between several close wells (PN junction) or from edge regions thereby enabling the device to serve a number of electrical functions without involving any special logical or circuit solutions (paragraph: 0045).

With respect to claim 8, Japanese Patent Application Laid-Open No. 9-283716 (1997) made obvious wherein said fourth impurity region is depleted in its entirety when a PN junction between the said fourth impurity and said semiconductor layer is subjected to application of a reverse voltage (Similar structure and similar function; the reference could be fully depleted if it had a large enough reverse voltage).

With respect to claim 9, Japanese Patent Application Laid-Open No. 9-283716 (1997) is silent on further comprising a second trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said

second trench isolation structure and said first impurity region together defining a second trench isolation region in said RESURF isolation region, and

a second MOS transistor, comprising

a fourth impurity region of said second conductivity type provided in said upper surface of said semiconductor layer defined in said second trench isolation region, said fourth impurity region being connected to a drain electrode of said second MOS transistor,

a fifth impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and fourth impurity regions, and

a second source region of said second conductivity type provided in an upper surface of said fifth impurity region.

As discussed in claim 1, all structural limitation for a first MOS transistor was specified in the same semiconductor layer.

Also the Japanese Patent Application Laid-Open No. 9-283716 (1997) also teaches a two MOS structure as shown in Figure 7.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine structure as indicated in claim 1 and the Japanese Patent Application Laid-Open No. 9-283716 (1997) structure of Figure 7 to have claimed structure (using a second MOS transistor with the same structural limitation as claim 1) for shielding same structural adjacent components together.

5) Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent Application Laid-Open No. 9-283716 (1997) and Wada (US 6274919) and further in view of Stengl (US 5113237).

With respect to claim 10, all reference to claim 1 is discussed above and the Japanese Patent Application Laid-Open No. 9-283716 (1997) discloses in Figure 12, "an interconnect line (8) provided over said first trench isolation structure (see claim 1) to be electrically connected to said drain electrode (8), and a field plate (11) held between said first trench isolation structure and said interconnect line (8), wherein said field plate (11) is a floating electrode."

The Japanese Patent Application Laid-Open No. 9-283716 (1997) was silent on the field plate being an electrode which is electrically connected to said semiconductor layer (2) defined in said first trench isolation region, or an electrode which is electrically connected to said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region.

Stengl (US 5113237) teaches field plate application that controls high breakdown voltage to have a structure as shown in Figure 1 that comprises a field plates (11,12,13,14,15) that high voltage that causes electric field between the surface and the pn-junction takes place evenly and, accordingly, a relatively even field distribution prevails. The large-area covering the border region of the pn-junction by the field plates, which only leave narrow gaps between, them, has the effect that a high breakdown voltage can be achieved with that structure (Col. 4: lines 41-68).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to take the teachings of Stengl (US 5113237) as seen in Figure 1 and combine it to the Japanese Patent Application Laid-Open No. 9-283716 (1997) as discussed in claim 1 to have a field plate structure to meet the claimed structure so as to achieved a structure that covers a large area between the field plates and the pn-junction to attain a high-breakdown voltage structure (Col. 4: lines 41-68).

6) Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent Application Laid-Open No. 9-283716 (1997), Wada (US 6274919) and Leonardi (US 2002/0008299) and further in view of Stengl (US 5113237).

With respect to claim 11, Japanese Patent Application Laid-Open No. 9-283716 (1997) discloses in Figure 12, "a second insulating film (7) provided on said semiconductor layer (2) defined between said first impurity region (3) and said buried impurity region (4)."

The Japanese Patent Application Laid-Open No. 9-283716 (1997) based on claim 3 is silent on [a plurality of field plates provided on said second insulating film (7), wherein said plurality of conductive films are exposed from said upper surface of semiconductor layer, and wherein said plurality of field plates are respectively connected to said plurality of conductive.

Stengl (US 5113237) teaches field plate application that controls high breakdown voltage to have a structure as shown in Figure 1 that comprises a field plates (11,12,13,14,15) that high voltage that causes electric field between the surface and the

pn-junction takes place evenly and, accordingly, a relatively even field distribution prevails. The large-area covering the border region of the pn-junction by the field plates, which only leave narrow gaps between, them, has the effect that a high breakdown voltage can be achieved with that structure (Col. 4: lines 41-68).

Claim 3 above has all the discussions and motivation about plurality of conductive films.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Stengl (US 5113237) and apply it to the teachings as discussed in claim 3 to form the claimed structure so as to achieved a structure that covers a large area between the field plates and the pn-junction to attain a high-breakdown voltage structure (Col. 4: lines 41-68).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark D. Pe whose telephone number is (571)272-0237. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571)272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDP

GEORGE ECKERT
PRIMARY EXAMINER